

DATA SHEET

TDA3567 NTSC decoder

Product specification
File under Integrated Circuits, IC02

June 1986

NTSC decoder**TDA3567****GENERAL DESCRIPTION**

The TDA3567 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Further more it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	pin 1	$V_P = V_{1-17}$	9	12	13,2	V
Supply current	pin 1	$I_P = I_1$	—	65	—	mA
Luminance input signal	pin 8					
Input voltage						
(peak-to-peak value)		$V_{8-17(p-p)}$	—	0,45	—	V
Contrast control range			—	20	—	dB
Chrominance amplifier	pin 3					
Input voltage						
(peak-to-peak value)		$V_{3-17(p-p)}$	—	550	—	mV
Saturation control range			50	—	—	dB
RGB matrix and amplifiers						
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)		$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Sandcastle input	pin 7					
Blanking input voltage		V_{7-17}	1,0	1,5	2,0	V
Burst gating and clamping input voltage		$V_{7-17(p-p)}$	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heatspreader (SOT102-1); SOT102-1; 1996 November 25.

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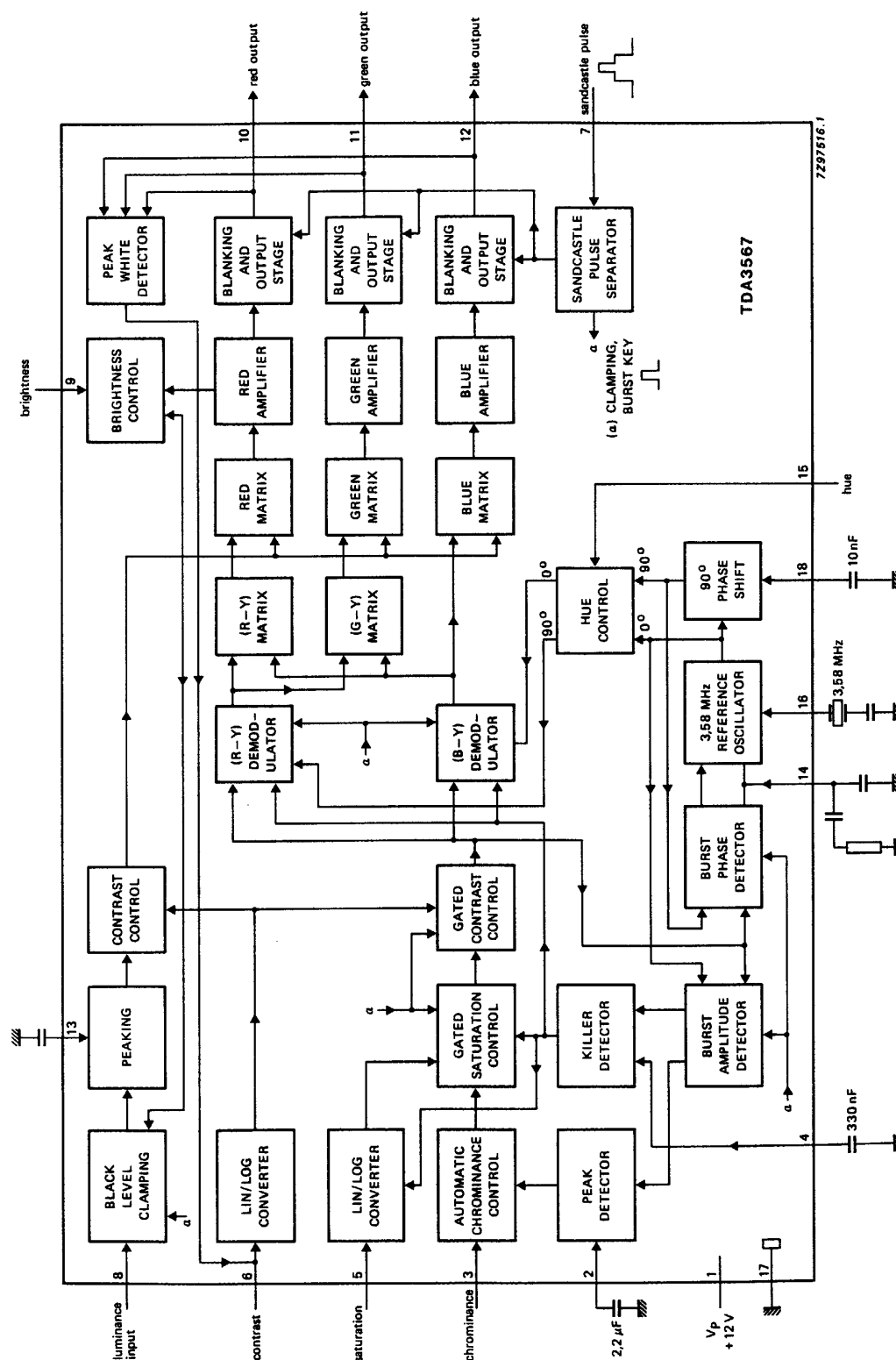


Fig.1 Block diagram.

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FUNCTIONAL DESCRIPTION**Luminance amplifier**

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak ⁽¹⁾ The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal must be a.c. coupled to the input pin 8.

The black level clamp circuit of the RGB amplifiers uses the coupling capacitor as a storage capacitor. After clamping the signal is fed to a peaking stage. The RC network connected to pin 13 is used to define the amount of overshoot.

The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to pin 6. The control voltage range is nominally -17 to +3 dB. The linear curve of the contrast control voltage is shown in Fig.2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal at pin 3 must be a.c. coupled, and must have an amplitude of 550 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal should not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via pin 5. The control voltage range is 2 V to 4 V. The impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase and a.c.c. detectors.

Oscillator and a.c.c. circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between pin 16 and ground. The oscillator does not require adjustment due to the small spreads of the IC. The free running frequency of the oscillator can be checked by connecting the saturation control (pin 5) to the positive supply line. Then the loop is opened, so that the frequency can be measured. The oscillator has an internal gain limiting stage which controls the gain to unity, so that internal signals are sinusoidal. This prevents the generation of higher harmonics of the subcarrier signals. The burst signal is compared to a 0° reference signal by the burst amplitude detector and is then amplified and fed to a peak detector for a.c.c. and to a sample and hold circuit which drives the colour killer circuit. The reference signal for the burst phase detector is provided by the 90° phase shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing oscillator signals with a phase of 0° and 90° before they are fed to the (R-Y) and (B-Y) demodulators. The 90° phase shifted signal is provided by a miller integrator (biased by pin 18). As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals are obtained from the hue control circuit. In nominal hue control position the phase angle of (R-Y) reference signal is 0°, the phase angle of the (B-Y) reference signal is 90°.

For flesh tone corrections the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$$(R - Y)_{\text{matrixed}} = 1,61 (R - Y)_{\text{IN}} - 0,42 (B - Y)_{\text{IN}}$$

$$(G - Y)_{\text{matrixed}} = 0,43 (R - Y)_{\text{IN}} - 0,11 (B - Y)_{\text{IN}}$$

$$(B - Y)_{\text{matrixed}} = (B - Y)_{\text{IN}}$$

(1) Signal with negative going sync; amplitude includes sync pulse amplitude.

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In these equations $(R-Y)_{IN}$ and $(B-Y)_{IN}$ indicate the colour difference signal amplitudes, when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90° and a gain ratio $B-Y/R-Y = 1,78$.

RGB matrix circuit and amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst-to-chrominance ratio of the input 1 : 2.2)
- Contrast –3 dB (maximum)
- Saturation –10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak). The black level of the red channel is compared with a variable external reference level (pin 9), which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level control, therefore the green and blue outputs will follow any variation of the red output. The output of the black control can be varied between 2 V to 4 V. The corresponding brightness control voltage is shown in Fig.4.

If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}	–25 to	+ 150	° C
Operating ambient temperature range	T_{amb}	–25 to	+ 65	° C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50	K/W
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CHARACTERISTICS

 $V_P = V_{1-17} = 12\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply voltage		$V_P = V_{1-17}$	9	12	13,2	V
Supply current		$I_P = I_1$	–	65	–	mA
Total power dissipation		P_{tot}	–	0,78	–	W
Luminance input signal						
Input voltage (peak-to-peak value)	note 1 pin 8	$V_{8-17(p-p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_{8-17}	–	–	1	V
Input current		I_8	–	0,15	1,0	µA
Contrast control range	see Fig.2		–17	–	+3	dB
Input current contrast control	for $V_{6-17} < 6\text{ V}$	I_7	–	0,5	15	µA
Input current when the peak-white limiter is active	$V_{6-17} = 2,5\text{ V}$	I_7	–	5,5	–	mA
Input resistance	$V_{6-17} > 6\text{ V}$	R_{7-17}	1,4	2,0	2,6	kΩ
Peaking of luminance signal						
Output impedance	pin 13	$ Z_{13-17} $	–	200	–	Ω
Ratio of internal/external current when pin 13 is short-circuited			–	3	–	

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Chrominance amplifier						
Input signal amplitude (peak-to-peak value)	note 2 pin 3	$V_{3-17(p-p)}$	—	550	—	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3-17(p-p)}$	—	—	1,1	V
Minimum burst signal amplitude within the a.c.c. control range (peak-to-peak)			35	—	—	mV
A.C.C. control range			30	—	—	dB
Change of the burst signal at the output for the complete control range		ΔV	—	—	+1	dB
Input impedance	pin 3	$ Z_{3-17} $	6	8	10	k Ω
Input capacitance	pin 3	C_{3-17}	—	4	6	pF
Saturation control range	see Fig.3		50	—	—	dB
Input current saturation control	for $V_{5-17} > 6\text{ V}$	I_5	—	1	20	μA
Input impedance	$V_{5-17} = 6\text{ V}$ to 10 V	$ Z_{5-17} $	1,4	2,0	2,6	k Ω
Input impedance when the colour killer is active		$ Z_{5-17} $	1,4	2,0	2,6	k Ω
Input impedance	for $V_{5-17} > 10\text{ V}$	$ Z_{5-17} $	0,7	1,0	1,3	k Ω
Tracking between luminance and chrominance contrast	for 10 dB of control		—	1	2	dB
Cross coupling between luminance and chrominance amplifier	note 4		—	—50	—46	dB

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reference part						
Phase locked loop						
Catching range		Δf	± 400	± 500	–	Hz
Phase shift for 400 Hz deviation of the carrier frequency		Δ	–	–	5	deg
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	$\Delta V_P = \pm 10\%$	Δf_{osc9}	–	150	250	Hz
Input resistance	pin 16	R_{16-17}	260	360	460	Ω
Input capacitance	pin 16	C_{22-17}	–	–	10	pF
A.C.C. generation						
Voltage at pin 4 nominal input signal		V_{4-17}	–	4,0	–	V
Voltage at pin 4 without burst input		V_{4-17}	–	1,9	–	V
Colour-off voltage		V_{4-17}	–	2,5	–	V
Colour-on voltage		V_{4-17}	–	2,8	–	V
Change in burst amplitude with temperature			–	0,1	–	%/K
Change in burst amplitude with 10% supply voltage change			–	0	–	%/V
Voltage at pin 2 at nominal input signal		V_{2-17}	–	5,0	–	V
Hue control						
Control voltage range			see Fig.5			
Input current	for $V_{15-17} < 5\text{ V}$	I_{14}	–	0,5	20	μA
Input impedance	for $V_{15-17} > 5\text{ V}$	$ Z_{14-17} $	1,5	2,5	3,5	k Ω

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Demodulation part						
Ratio of demodulation signals (measured at the various outputs)	note 7					
(R-Y)/(B-Y); no (R-Y) signal		$\frac{V_{10-17}}{V_{12-17}}$	—	−0,42	—	
(R-Y)/(B-Y); colour bar signal		$\frac{V_{10-17}}{V_{12-17}}$	—	1,4	—	
(G-Y)/(R-Y); no (B-Y) signal		$\frac{V_{11-17}}{V_{12-17}}$	—	−0,25	—	
(G-Y)/(B-Y); no (R-Y) signal		$\frac{V_{11-17}}{V_{12-17}}$	—	−0,11	—	
Frequency response	0 to 0,7 MHz		—	—	−3	dB
RGB matrix and amplifier						
Output signal amplitude	at nominal luminance input signal and nominal contrast (peak-to-peak value) note 3 black-white	$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel	at nominal contrast and saturation control setting and no luminance signal to the input (B-Y) signal (peak-to-peak value)	$V_{12-17(p-p)}$	—	3,8	—	V
Maximum peak-white level	note 6	$V_{10,11,12-7}$	9,0	9,3	9,6	V
Maximum output current		$I_{10,11,12-17}$	—	—	10	mA
Difference in the black level between the three channels			—	—	600	mV
Black level shift with vision content			—	10	40	mV
Brightness control voltage range			see Fig.4			

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Brightness control input current		I_g	—	—	–50	μA
Black level variation with temperature		V/T	—	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	—	75	200	mV
Relative spread between the three output signals			—	—	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness ($\pm 1\text{ V}$), and supply voltage ($\pm 10\%$)	ΔV	—	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	—	0	20	mV
Blanking level at the RGB outputs		V_{b1}	1,95	2,15	2,35	V
Tracking of output black levels with supply voltage		$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_p}{\Delta V_p}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 5	S/N	62	—	—	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	—	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	—	50	75	mV
RGB output impedance		$ Z_{10,11,12-17} $	—	—	50	
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		—	—	–3	dB

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Sandcastle input						
Level at which the RGB blanking is activated		V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input currents	$V_{7-17} = 0 \text{ to } 1 \text{ V}$	I_7	–	–	–1	mA
	$V_{7-17} = 1 \text{ to } 8,5 \text{ V}$	I_7	–	–20	–40	μA
	$V_{7-17} = 8,5 \text{ to } 12 \text{ V}$	I_7	–	–	2	mA

Notes to the characteristics

- Signal with negative going sync; amplitude includes sync pulse amplitude.
- Indicated is a signal for colour bar with 75% saturation, so the chrominance to burst ratio is 2,2 : 1.
- Nominal contrast is specified as maximum contrast –3 dB and nominal saturation as maximum saturation –10 dB.
- Cross coupling is measured under the following condition:
 - input signals nominal;
 - contrast and saturation such that nominal output signals are obtained;
 - the signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
- The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise.
- When this level is exceeded the amplifier of the output signal is reduced via a discharge of the capacitor on pin 7 (contrast control). Discharge current is 5,5 mA.
- These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'.

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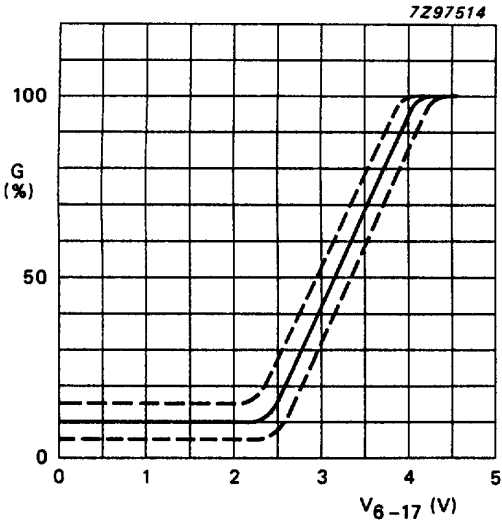


Fig.2 Contrast control voltage range.

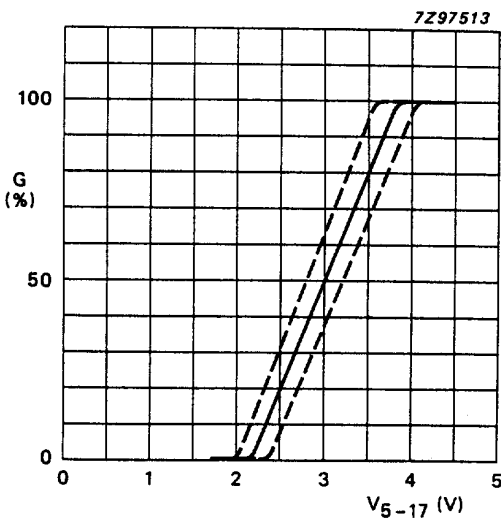


Fig.3 Saturation control voltage range.

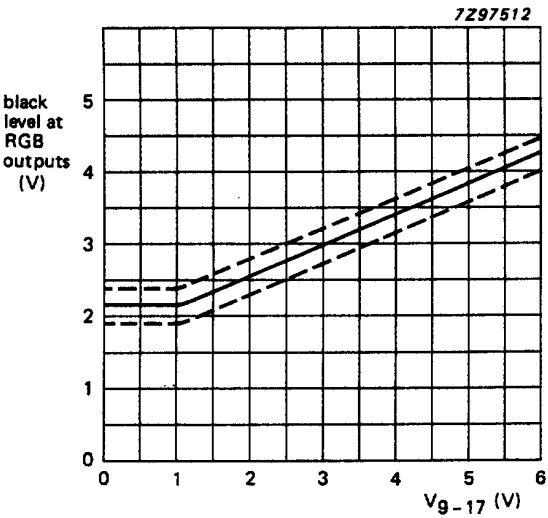


Fig.4 Brightness control voltage range.

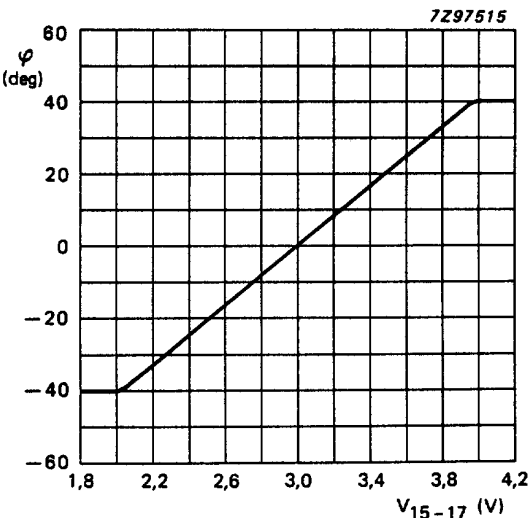


Fig.5 Hue control voltage range.

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APPLICATION INFORMATION

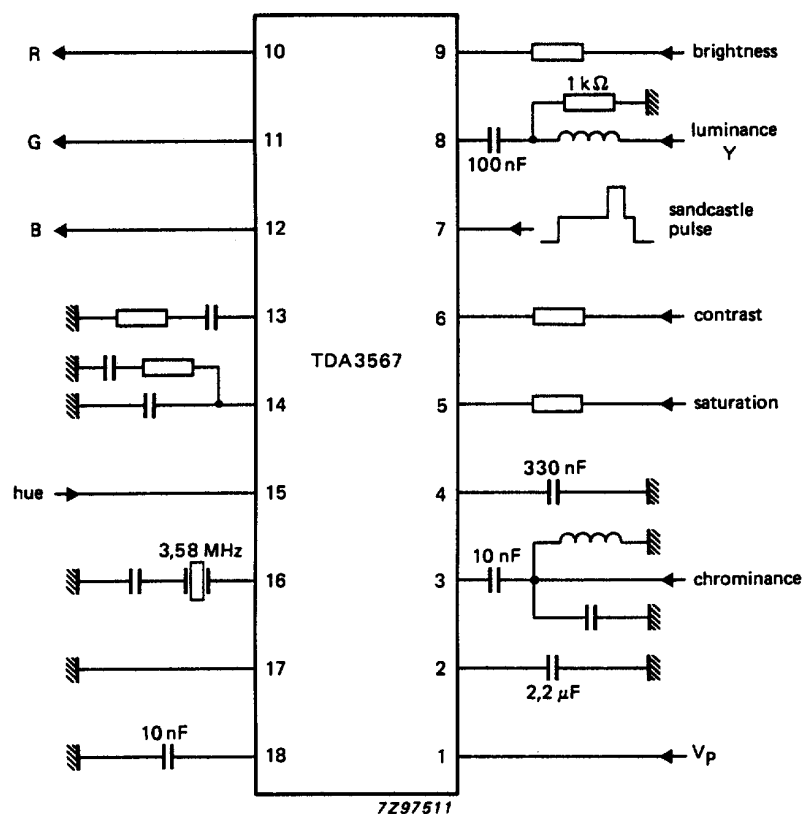


Fig.6 Application diagram.

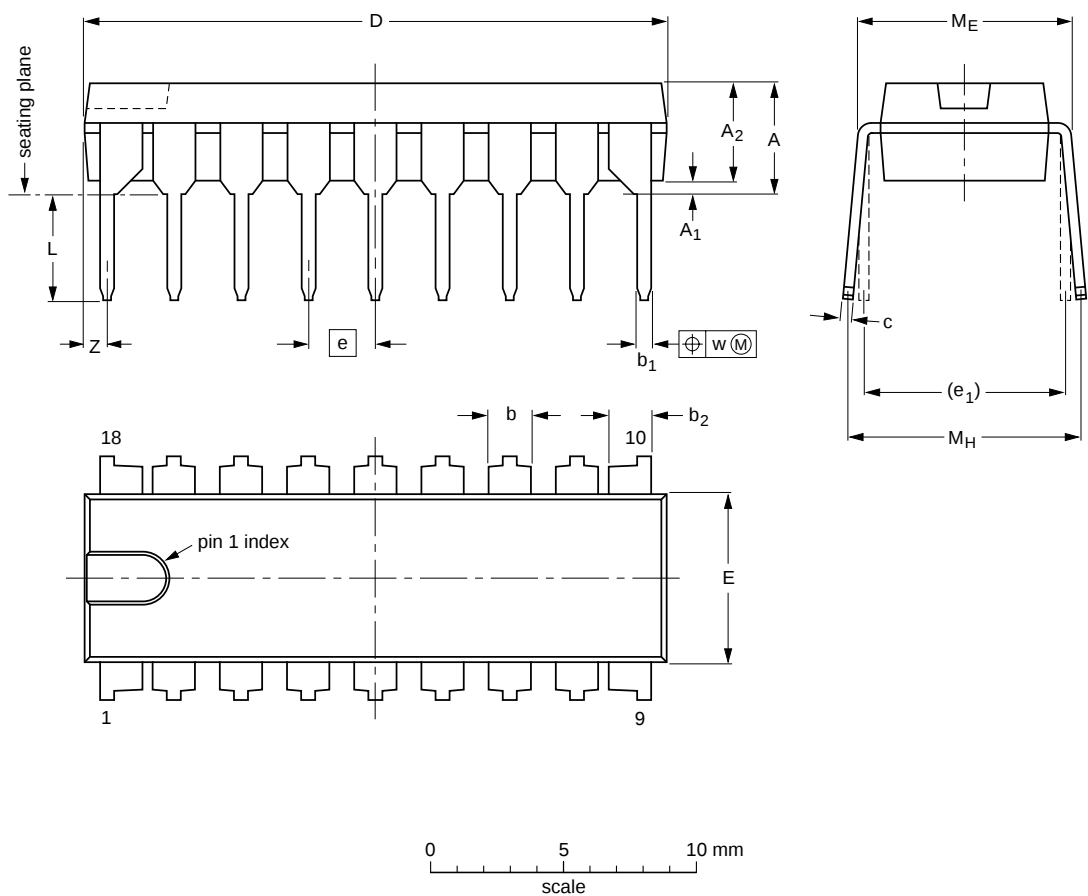
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PACKAGE OUTLINES

DIP18: plastic dual in-line package; 18 leads (300 mil)

SOT102-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						93-10-14 95-01-23

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SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.