

TV STEREO/DUAL SOUND IDENTIFICATION DECODER

The TDA2795 is a monolithic integrated circuit for stereo/dual sound in television receivers.

The circuit incorporates the following functions:

- Controlled pilot signal amplifier.
- Envelope demodulator.
- Two separate signal paths for processing the identification frequencies: operational amplifier for active filter, integral evaluation circuit with TTL compatible 'open collector' outputs.
- Stereo indicator driver.

QUICK REFERENCE DATA

Supply voltage	V_S	typ.	12 V
Supply current	I_S	typ.	8 mA
Nominal input voltage at $f = 54,6875$ kHz	V_i	typ.	10 mV
Input impedance	$ Z_i $	$\geq$	500 k Ω
Operational amplifier			
open loop voltage gain at 200 Hz	G_o	$\geq$	78 dB
input resistance	R_i	$\geq$	1 M Ω
output resistance	R_o	$\leq$	3,5 k Ω
Supply voltage range	V_S	10,8 to 13,2 V	
Operating ambient temperature range	T_{amb}	0 to + 70 °C	

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

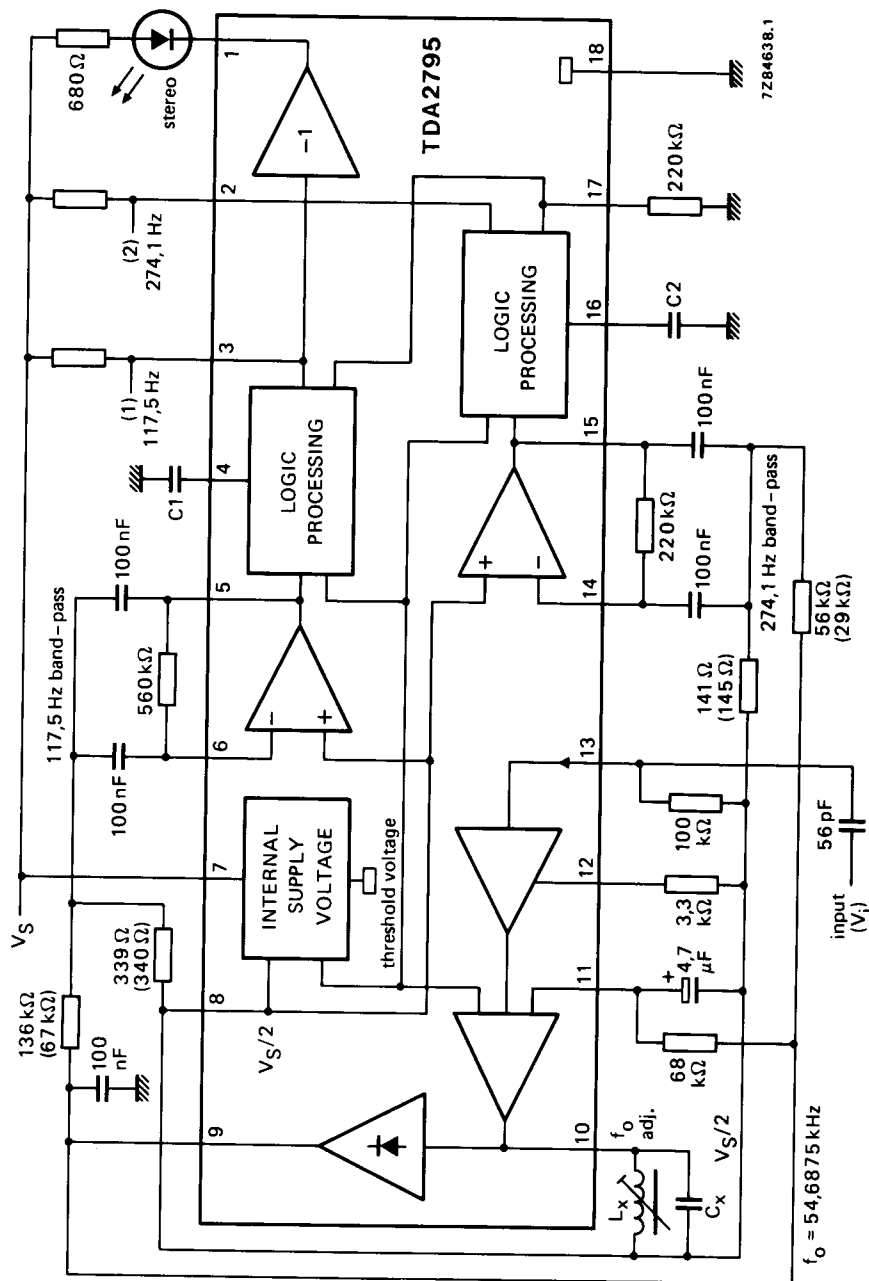


Fig. 1 Block diagram; C1 and C2 values 22 to 150 nF (dependent on switching time); values given in parenthesis are for $G = 4$ at 117.5/274.1 Hz; $C_x = 3.3$ nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_{7-18} = V_S$	max.	15 V
Signal input (pin 13)	V_{13-18}	max.	V_S V
	$-V_{13-18}$	max.	0,5 V
Switch outputs (pins 1, 2 and 3)	V_{1-18}	max.	18 V
	I_1	max.	50 mA
	$V_{2;3-18}$	max.	15 V
	$I_{2;3}$	max.	5 mA
	$-V_{1;2;3-18}$	max.	0,5 V
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}	-25 to +125 °C	
Operating ambient temperature range	T_{amb}	0 to +70 °C	

CHARACTERISTICS

$V_S = 12$ V; $T_{amb} = 25$ °C, unless otherwise specified; measured in Fig. 1, at $V_i = 10$ mV; $f = 54,6875$ kHz amplitude modulated with $f_{m1} = 117,5$ Hz or $f_{m2} = 274,1$ Hz; $m_1 = m_2 = 50\%$.

Supply voltage range	V_S	10,8 to 13,2 V
Supply current	I_S	typ. 8 mA ≤ 12 mA

Pilot signal amplifier and envelope demodulator

Maximum input voltage (peak-to-peak value)	$V_{i(p-p)}$	typ. 2 V
Input impedance	$ Z_{13-18} $	≥ 500 kΩ
Voltage gain (V_{9-18}/V_{13-18}) at $V_i = 1$ mV	G_{v9-13}	typ. 42 dB
Start of control at V_i	see Fig. 3	
Control range	ΔG_v	≥ 40 dB
Controlled output voltage (r.m.s. value) (pin 9)	$V_{o(rms)}$	typ. 550 mV

Operational amplifiers

Input bias current (pins 6 and 14)	$\pm I_{6;14}$	≤ 70 nA
Open loop voltage gain at $f = 200$ Hz	G_o	≥ 78 dB
Available output current (pins 5 and 15)	$\pm I_{5;15}$	≥ 1,5 mA
Output resistance (pins 5 and 15)	R_o	typ. 2 kΩ ≤ 3,5 kΩ
Allowable load capacitance	C_L	≤ 30 pF
Output offset voltage at $R_{5-6} = 560$ kΩ	$\pm V_{o5-8}$	≤ 70 mV

CHARACTERISTICS (continued)**Evaluation circuitry**

Switch-on threshold voltage (pins 5 and 15)

 $V_5; V_{15}$ typ. 1,0 V

Switch hysteresis

 $\frac{V_{5on}}{V_{5off}} = \frac{V_{15on}}{V_{15off}}$ typ. $3,8 \pm 0,5$ dB

Switch outputs (pins 2 and 3)

allowable output current

 $I_3; I_2 \leq 2$ mAsaturation voltage at $I_3 = I_2 = 1,5$ mA $V_{3;2-18sat} \leq 0,35$ Vleakage voltage at $I_3 = I_2 \leq 5$ μ A $V_{3;2-18} \leq 15$ V

Indicator driver (pin 1)

allowable output current

 $I_1 \leq 40$ mAsaturation voltage at $I_1 = 20$ mA $V_{1-18sat} \leq 0,8$ Vleakage voltage at $I_1 < 10$ μ A $V_{1-18} \leq 18$ V**Internal reference voltage**

Reference voltage (pin 8)

 V_{8-18} typ. 6 V

Available output current (pin 8)

 $-I_8 \geq 2$ mA
 $+I_8 \geq 0,6$ mA**Reference current source**

Reference voltage (pin 17)

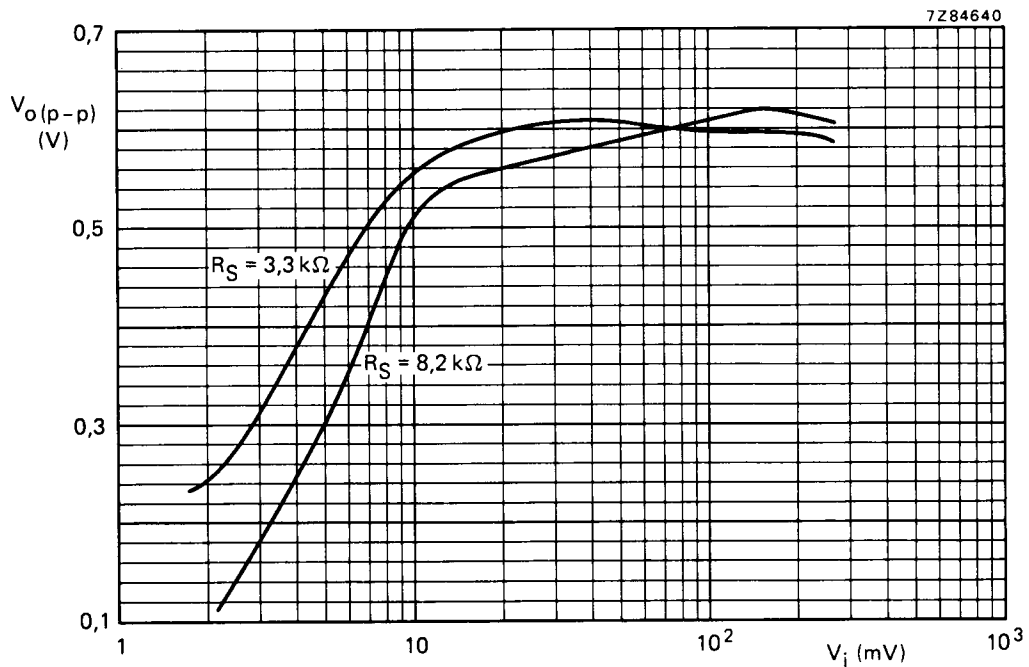
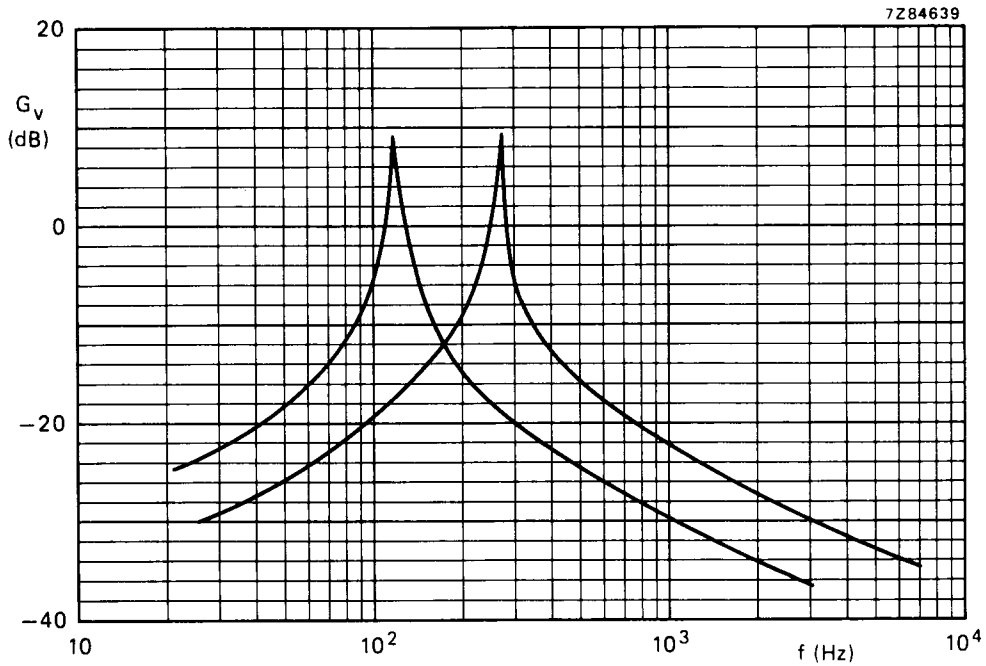
 V_{17-18} typ. 5,3 V

Internal bias resistor

 R_{i17} typ. 5 k Ω

Allowable load resistor (pin 17)

 R_L 180 to 270 k Ω

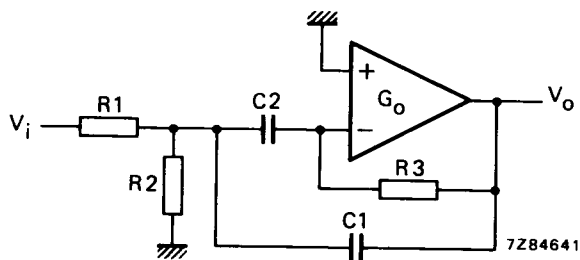


GENERAL FILTER CALCULATIONS

1. Gain

Amplifier conditions: $G_o \gg G_v$ and $G_o \gg 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p \frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}, \text{ in which: } p = j\omega; G_v = \frac{V_o}{V_i}$$



2. Resonance frequency

$$\omega_r = \frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$$

3. Gain at $\omega = \omega_r$

$$-G_{vr} = \frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$$

4. Quality

$$Q = \frac{\sqrt{C1 \cdot C2}}{C1 + C2} \cdot \sqrt{\frac{R3 (R1 + R2)}{R1 \cdot R2}}$$

5. Recommended components

C1 and C2: 5% MKC (metallized polycarbonate film capacitor)

R1, R2 and R3: 2% MR (metal film resistor)

or:

C1 and C2: 5% MKT (metallized polyester film capacitor)

R1, R2 and R3: 2% CR (carbon film resistor)